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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/554,219	08/14/2000	Kunio Minomiya	43890-416	6492

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McDermott Will & Emery
600 13th Street NW
Washington, DC 20005-3096

EXAMINER

NATNAEL, PAULO S M

ART UNIT	PAPER NUMBER
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2614

DATE MAILED: 04/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/554,219

Applicant(s)

NINOMIYA ET AL

Examiner

Paulos M. Natnael

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 February 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4,7,8 and 10 is/are rejected.
- 7) ☒ Claim(s) 2,3,5,6 and 9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1,4,7,11** rejected under 35 U.S.C. 102(b) as being anticipated by Krishamurthy et al. U.S. Pat. No. 5,508,748.

Considering claim 1, the claimed circuit for establishing the synchronous signal in reception data based on a polarity of the most significant bit (MSB) of the reception transport packet data is met by slicer and generator 36, Fig.5. (See also col. 6, lines 25-35 and 45-55)

Considering claim 4, wherein a differential value of synchronous signals of reception packet is determined so as to detect a clock phase error of transmission data, and the clock signal is regenerated by phase control on the basis of said clock phase error, is met by the disclosure that "Converter 38 further includes a divider 52 which is also reset by FSYNC to synchronize its operation with the beginning of each data frame 10. In particular, divider 52 is a divide-by-208 counter which is clocked by the Byte Clock generated by divider 50 to generate a Begin RS Block signal for identifying the beginning of each block of 208 data bytes synchronously with the first data byte of each

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data frame..." (Col. 9, lines 7-15) and "Also, by referencing the system to the highest byte clock rate, increased burst error protection will be provided as the VSB mode and the corresponding byte rate decrease, because the interleave pattern is effected over a given number of bytes regardless of VSB mode. (Col. 9, 41-45)

Considering claim 7, wherein the clock signal is regenerated by detecting a clock phase error from the differential value of the data coinciding with a synchronous signal code pattern of reception data until the synchronous signal of reception packet data is detected and established;

Regarding claim 7, see rejection of claim 4.

Considering claim 11, the claimed wherein said polarity of said polarity of the most significant bit (MSB) of the reception transport packet data is either positive or negative, is inherent, because by definition polarity of a given number, a data, is either negative or positive.

8. Claim **1 and 11** are rejected under 35 U.S.C. 102(b) as being anticipated by Citta et al. , U.S. Pat. No. 5,602,595.

Considering claim 1, Citta discloses all claimed subject matter, note;

a) the claimed circuit for establishing the synchronous signal in reception data, is met by Sync and Timing circuit 42 (Fig.4), which detects "data segment syncs...from the synchronously detected random data". (col. 3, lines 49-50).

b) the claimed based on a polarity of the most significant bit (MSB) showing the positive or negative sign of the reception transport packet data" is inherent because for example Citta is manipulating or processing the bytes of the Header data from 4 bytes to 3 bytes in the MPEG transport Packet w/o Sync (FIG. 3B).

Considering claim 11, the claimed wherein said polarity of said polarity of the most significant bit (MSB) of the reception transport packet data is either positive or negative, is inherent, because by definition polarity of a given number, a data, is either negative or positive.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Citta et al., U.S. Pat. No. 5,602,595.

Considering claim 8, wherein a synchronous signal in the received packet data is detected, the difference between the detected data value of the synchronous signal and a predetermined reference is value determined, and automatic gain control is performed on the basis of this difference.

Regarding claim 8, Citta does not specifically disclose AGC realization based on the difference between the detected data value and the reference signal. However, Examiner here takes Official Notice in that it is well known in the art that signal gain is automatically controlled within specified limits with respect to a reference frequency or value and, thus, it would have been obvious to those with ordinary skill in the art at the time the invention was made to modify the system of Citta and provide it with an AGC signal in order to maintain the overall gain of the system at a constant or desired level.

Considering claim 10, wherein automatic gain control is performed by detecting the amplitude difference from an envelope of analog detected base band signal until a synchronous signal of reception packet data is detected and established.

Regarding claim 10, see rejection of claim 8.

Response to Arguments

Applicant's Arguments

a) It does not appear that the circuit 36 of Krishnamurthy, which is illustrated in detail in Fig.5, utilized or considers the most significant bit (MSB) of the reception transport packet data when establishing the synchronous signal. It is further noted that the portions of Krishnamurthy cited in the pending rejection also fail to mention or suggest utilization of the polarity of the MSB of the transport packet data to establish the synchronous signal...for the foregoing reasons, Krishnamurthy does not anticipate claim 1.

b) As such, the divider of Krishnamurthy cannot be properly relied upon as disclosing the present invention as recited by claim 4. Thus, it is respectfully submitted that claim 4 is not anticipated by Krishnamurthy.

c) Finally, it is noted that for at least the same reasons of claim 4, Krishnamurthy also fails to anticipate claim 7.

d) However, it does not appear that the circuit 42 of Citta utilized or considers the polarity the most signal bit (MSB) of the reception transport packet data when establishing the synchronous signal.

e) First, Applicants are not merely attempting to claim AGC as novel. It is the combination of the generation of the difference signal (which is based on the difference between the synchronous signal and the reference value) and the utilization of this difference signal to perform the AGC in a digital broadcast demodulator that the

Applicants believe to be novel. Second, it does not appear that Citta even discloses the generation of the claimed difference signal. Thus, as each and every limitation of the pending claim must be disclosed or suggested by the prior art in order to establish a prima facie case of obviousness...and for at least the foregoing reasons, Citta fails to do so, it is respectfully submitted that claim 8 is patentable over Citta.

Examiner Response

a) The claimed invention discloses (in page 8) that when processed by the complement of 2, the codes of the segment of the synchronous signal show a changed polarity. Fig. 4A of Krishnamurthy discloses the ranges of symbol levels in two's complement. Fig. 4A shows the positive and negative ranges of the VSB symbols. And Krishnamurthy further discusses fig.4 and discloses, "This 9-bit signal is illustrated in FIG. 4A for each of the four VSB modes. It will be observed that the four most significant bits (MSB's) of each 9-bit symbol, with the MSB inverted, represent, for VSB mode M=16, the four data bits corresponding to the respective symbol." Here Krishnamurthy is clearly discussing the changes of the polarity of the four-bit MSB when processed in two's complement. Therefore, the argument that the Krishnamurthy does not appear that the circuit 36 of Krishnamurthy utilized or considers the most significant bit (MSB) of the reception transport packet data when establishing the synchronous signal, is unpersuasive to say the least.

b) see rejection of part A.

c) see rejection of claim A.

d) Fig.1 of Citta discloses the MPEG standard data frame, which comprises two data fields of 313 data segments each, with each data segment comprising 832 multilevel symbols. (Example of Multilevel symbols are illustrated in Fig. 4A of Krishnamurthy). The first data segment in each field comprises a data field sync segment and each data segment is headed by a four symbol data segment sync followed by 828 data and FEC (forward error detection) symbols. (col. 1 lines 30-40) Thus, the multi-level symbols take the polarity of the MSB in consideration. In other words, the synchronous signals are processed based on the polarity of the MSB in the packet data. Argument therefore is not considered persuasive.

e) Again, it is well known in the art to realize the AGC by detecting the difference between data value of the synchronous signal and some predetermined reference is value is determined, i.e., signal gain is automatically controlled within specified limits with respect to a reference frequency or value and, thus, it would have been obvious to those with ordinary skill in the art at the time the invention was made to modify the system of Citta and provide it with an AGC signal in order to maintain the overall gain of the system at a constant or desired level. Argument is not persuasive.

Allowable Subject Matter

11. Claims **2,3,5,6, and 9** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a digital broadcast demodulator comprising a synchronous code pattern detecting circuit for detecting the segment synchronous code pattern from the most significant bit signal of the reception packet data, a symbol number counter for counting the number of symbol data in the reception packet data, a synchronous detection circuit for judging the true segment synchronous code pattern by obtaining the segment synchronous code pattern from said synchronous code pattern detecting circuit when said symbol number counter finishes counting of a specified number, and a synchronism detection protection counter for detecting and establishing the segment synchronous signal in the reception data from the output of said synchronous code pattern detecting circuit and count-up of specified number of said symbol number counter, as in claim 2;

Wherein the most significant bit signal of the reception packet data is processed so as to issue a signal showing the start position of the synchronous signal in the data and a signal of detecting and establishing the synchronous signal, as in claim 3;

A clock phase error detecting circuit for issuing a clock phase error of transmission data by determining the difference of the N-th and N+1-th ($N > 1$)

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synchronous signals which should be of same level by nature, from the code pattern detection signal of synchronous signal and signal showing position of synchronous signal, as in claim 5;

A circuit for processing the difference of all reception data, a circuit for detecting the differential value only for the data coinciding with the code pattern of synchronous signal, and
a circuit for detecting the differential value only for the data of synchronous signal, as in claim 6;

An AGC error detecting circuit for detecting a specific position of synchronous signal from the signal showing detection and establishment of synchronous signal in the reception data and the signal showing position of synchronous signal, and issuing the error of the synchronous signal at this specific position and the reference value as a control signal, as in claim 9.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chen, U.S. Pat. No. 6,160,543 discloses a transmission device for computer video signals comprising a polarity separating circuit 11 and polarity mode generating circuit 12 that monitor the polarity of the input synchronous signal.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 6:30am -3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

Paulos Natnael
April 18, 2003



JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600